

13. A liquid crystal display comprising:

an insulating substrate;

a gate wire and a data wire insulated from each other over the substrate, the gate wire including pluralities of gate lines and gate pads, and the data wire including pluralities of data lines and data pads;

a plurality of thin film transistors, each having a drain electrode and a source electrode electrically connected to the data line;

a passivation layer covering the gate wire, the data wire and the thin film transistors and having first, second and third contact holes which expose the gate pad, the data pad and the drain electrode at least in part, respectively;

a pixel electrode on the passivation film; the pixel electrode connected to the drain electrode through the third contact hole and overlapping at least a part of the data lines adjacent to the pixel electrode;

a first conductor on the passivation film, the first conductor connected to the gate pad through the first contact hole; and

a second conductor on the passivation film, the second conductor connected to the data pad through the second contact hole.

14. The liquid crystal display of claim 13, wherein the pixel electrode overlaps at least a part of the gate lines adjacent to the pixel electrode.

15. The liquid crystal display of claim 14, wherein all edges of the pixel electrode overlap the gate lines or the data lines adjacent to the pixel electrode.

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16. The liquid crystal display of claim 13, wherein at least an overlapping portion between the pixel electrode and the gate lines has larger width than other overlapping portions between the pixel electrode and the gate lines or the data lines.

17. The liquid crystal display of claim 13, wherein the first and the second conductors and the pixel electrode comprise the same material.

18. The liquid crystal display of claim 17, wherein the pixel electrode comprises a transparent conducting material.

19. The liquid crystal display of claim 17, wherein the pixel electrode comprises ITO.

20. The liquid crystal display of claim 13, further comprising a storage electrode electrically connected to the pixel electrode, the storage electrode including a layer different from the pixel electrode and serving as a terminal of a storage capacitor.

21. The liquid crystal display of claim 20, further comprising a storage line insulated from the storage electrode and overlapping the storage electrode to form another terminal of the storage capacitor.

22. The liquid crystal display of claim 21, wherein the storage electrode has width smaller than width of the storage line.

23. The liquid crystal display of claim 21, wherein the storage line and the gate lines comprise the same material.

24. The liquid crystal display of claim 13, wherein the storage electrode and the data lines comprise the same material.

25. The liquid crystal display of claim 24, wherein the passivation layer further has a fourth contact hole exposing the storage electrode, and the storage electrode is connected to the pixel electrode through the fourth contact hole.

26. The liquid crystal display of claim 13, wherein the thin film transistor further comprises a gate electrode connected to the gate line, a semiconductor layer insulated from the gate electrode, and a doped semiconductor layer on the semiconductor layer, the doped semiconductor layer being in contact with the source electrode and the drain electrode.

27. The liquid crystal display of claim 26, wherein entire portions of the doped semiconductor layer directly contact the semiconductor layer.

28. The liquid crystal display of claim 26, further comprising a gate insulating layer disposed between the gate wire and the data wire.

29. The liquid crystal display of claim 28, wherein at least a part of the data wire is in direct contact with the gate insulating layer.

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30. A liquid crystal display comprising:

an insulating substrate;

pluralities of gate lines and data lines insulated from each other over the substrate;

a plurality of thin film transistors, each having a drain electrode and a source electrode electrically connected to the data line;

a passivation layer covering the gate lines, the data lines and the thin film transistors, the passivation layer having a first contact hole which expose the drain electrode at least in part;

a pixel electrode on the passivation film, the pixel electrode connected to the drain electrode through the first contact hole, overlapping a part of the data lines adjacent to the pixel electrode; and

a first conductor including a layer different from the pixel electrode, electrically connected to the pixel electrode and serving as a terminal of a storage capacitor.

31. The liquid crystal display of claim 30, further comprising a second conductor insulated from the first conductor and overlapping the first conductor to form another terminal of the storage capacitor.

32. The liquid crystal display of claim 31, wherein the first conductor has width smaller than width of the second conductor.

33. The liquid crystal display of claim 31, wherein the second conductor and the gate lines comprise the same material.

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34. The liquid crystal display of claim 30, wherein the first conductor and the data lines comprise the same material.

35. The liquid crystal display of claim 34, wherein the passivation layer further has a second contact hole exposing the first conductor, and the first conductor is connected to the pixel electrode through the second contact hole.

36. The liquid crystal display of claim 30, wherein the pixel electrode overlaps at least a part of the gate lines adjacent to the pixel electrode.

37. The liquid crystal display of claim 36, wherein all edges of the pixel electrode overlap the gate lines or the data lines adjacent to the pixel electrode.

38. The liquid crystal display of claim 30, wherein at least an overlapping portion between the pixel electrode and the gate lines has larger width than other overlapping portions between the pixel electrode and the gate lines or the data lines.

39. The liquid crystal display of claim 30, wherein the thin film transistor further comprises a gate electrode connected to the gate line, a semiconductor layer insulated from the gate electrode, and a doped semiconductor layer on the semiconductor layer, the doped semiconductor layer being in contact with the source electrode and the drain electrode.

40. The liquid crystal display of claim 39, wherein entire portions of the doped semiconductor layer directly contact the semiconductor layer.

41. The liquid crystal display of claim 39, further comprising a gate insulating layer disposed between the gate lines and the data lines.

42. The liquid crystal display of claim 41, wherein at least a part of the data lines is in direct contact with the gate insulating layer.

43. A liquid crystal display comprising:

an insulating substrate;

a gate line on the insulating substrate;

a data line on the insulating substrate;

a thin film transistor on the insulating substrate wherein the thin film transistor comprises a pair of source/drains wherein a first of the pair of source/drains is coupled to the data line;

a passivation layer on the gate line, on the data line, and on the thin film transistor so that the gate line, the data line, and the thin film transistor are between the insulating substrate and the passivation layer wherein the passivation layer has a contact hole therein exposing a portion of a second of the pair of source/drains of the thin film transistor; and

a pixel electrode on the passivation layer so that the passivation layer is between the pixel electrode and the insulating substrate wherein the pixel electrode is coupled with the second of the pair of source/drains of the thin film transistor through the contact hole in

the passivation layer and wherein the pixel electrode extends onto a portion of the data line so that the portion of the data line is between the pixel electrode extending thereon and the insulating substrate.

44. The liquid crystal display of Claim 43 wherein the thin film transistor comprises a semiconductor layer and wherein the semiconductor layer includes the pair of source/drains, the liquid crystal display further comprising:

a gate insulating layer between the semiconductor layer and the gate line.

45. The liquid crystal display of Claim 44 wherein the pixel electrode extends onto a portion of the gate line without extending across the gate line so that the portion of the gate line is between the pixel electrode extending thereon and the insulating substrate.

46. The liquid crystal display of Claim 44 wherein the gate line and the data line cross, the liquid crystal display further comprising:

an insulating layer between the gate line and the data line at the crossing thereof.

47. The liquid crystal display of Claim 46 wherein the insulating layer between the gate line and the data line and the gate insulating layer each comprise a same material and have a same thickness.

48. The liquid crystal display of Claim 47 wherein the insulating layer between the gate line and the data line and the gate insulating layer comprise a same continuous layer.

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49. The liquid crystal display of Claim 43 further comprising:

a storage electrode between the insulating substrate and the passivation layer
wherein the passivation layer includes a second contact hole therein exposing a portion of
the storage electrode and wherein the pixel electrode is coupled with the storage electrode
through the second contact hole.

50. The liquid crystal display of Claim 49 further comprising:

a storage line between the storage electrode and the insulating substrate.

51. The liquid crystal display of Claim 50 further comprising:

an insulating layer between the storage line and the storage electrode.

52. The liquid crystal display of Claim 50 wherein the storage line is parallel to the

gate line and wherein the storage line crosses the data line wherein the storage line and
the data line are electrically insulated at the crossing thereof.

53. The liquid crystal display of Claim 49 wherein the gate line is between the

storage electrode and the insulating substrate.

54. The liquid crystal display of Claim 53 further comprising:

an insulating layer between the gate line and the storage electrode.

55. The liquid crystal display of Claim 43 further comprising:

a second gate line on the insulating substrate wherein the first and second gate lines do not cross; and

a second data line on the insulating substrate wherein the first and second data lines do not cross, wherein the first and second gate lines each cross the first and second data lines, wherein the gate lines and data lines are electrically insulated at the crossings thereof, and wherein each of the first and second gate and data lines is between the passivation layer and the insulating substrate.

56. The liquid crystal display of Claim 55 wherein the pixel electrode extends onto portions of each of the first and second gate and data lines.

57. The liquid crystal display of Claim 55 wherein the pixel electrode extends onto portions of each of the first and second gate and data lines without extending across any of the first and second gate and data lines.

58. The liquid crystal display of Claim 43 wherein the pixel electrode does not extend across the data line.

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